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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,142	03/25/2002	Timothy S. Lehner		2716

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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,142	LEHNER ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7,8,10,12,13,16,18,19 and 21-27* is/are pending in the application.

4a) Of the above claim(s) *21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7,8,10,12,13,16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *21-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in office action of 9 August 2005. Applicants' response on 9 November 2005 has amended claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19; presented new claims 21-27; and cancelled claims 2-3, 6, 9, 11, 14-15, 17, and 20.

Claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19, and 21-27 are pending in this application. Claims 1, 4-5, 7-8, 10, 12-13, 16, 18-19 have been rejected. Claims 21-27 are subject to a restriction requirement.

Restriction

1. Newly submitted claims 21-27 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 21-22 are directed to "a behaviorally equivalent circuit" which is separate and distinct from every previously presented claim. While it is conceivable that the invention of claims 21-22 could define a circuit within the meaning of the originally presented claims, none of the originally presented claims recite limitations that establish any substantial relationship between those claims and 21-22. In addition, the originally presented claims are properly classified in 703/14, "Circuit Simulation," newly presented claims 21-22 are properly classified in 703/20, "Target Device."

In addition, the originally presented claims are properly classified in 703/14, "Circuit Simulation," newly presented claims 21-22 are properly classified in 703/20, "Target Device."

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Claims 23-27 are directed to "a methodology for modeling and simulating a circuit" which is separate and distinct from every previously presented claim. Inasmuch as "a methodology" should be interpreted as "a method" and thus may be reasonably classified with the originally presented claims, the limitations of at least claim 23 are separate and distinct from every originally presented claim. For example, none of the originally presented claims make any requirement for "an ODE," "an ODE solver," or "solving said ODE," as recited by claim 23. Claim 23 contains no requirement of "an API," as recited by each originally presented independent claim.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 21-27 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Specification

The substitute specification filed on 9 November 2005 has been entered. The previous objections to the specification have been withdrawn.

The previous objections to the abstract have been withdrawn in light of the amendments thereto.

Drawings

The proposed drawings submitted on 9 November 2005 have been reviewed and found acceptable.

Claim Objections

The previous objection to claim 1 has been withdrawn in light of the amendments thereto.

The phrase "API" appearing throughout the claims will be interpreted as meaning "application programming interface."

The claims are generally replete with ambiguous language that makes it difficult to determine what Applicants regard as the invention.

Among the recurring issues in the claims are mixtures of apparatus-type and process-type limitations which make it difficult to determine the metes and bounds of the claimed invention. According to MPEP 2114:

> While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device

> *does.*" *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

For example, claims 4, 5, and 7 appear to recite method steps but depend from claim 1 which defines an apparatus. Applicants are respectfully encouraged to clearly define the invention(s) as falling into a single category of statutory invention per claim tree.

In claim 1, the meaning of the limitation "a simulator module comprising an API wherein said API comprises at least one function and wherein said simulator module uses said function to define a first circuit wherein said function is recorded" is unclear at best. The language of the claim appears to require a function, which exists prior to and defines a circuit, and the function is subsequently stored "within" the circuit. The precise meaning of this language is unknown. The Examiner speculates that the intended meaning of the claim is that the first circuit represents an implementation of the function (such as a full adder circuit implements an abstract addition function), but this is merely speculation. Does this step create a copy of the "at least one function" stored within the circuit?

In claim 1, the limitation "a code module which comprises a compilation of a plurality of said recorded functions" does not specifically correspond with the surrounding claim language. The apparent antecedent basis for "recorded functions" is "at least one function [which is] recorded," however this limitation calls for "a plurality of said recorded functions." It appears that antecedent basis for "a plurality of recorded functions" is required and should be explicitly recited.

This limitation is further confusing because it is unclear what definition of "compilation" should be inferred from the claim language. In the context of computer software, which ostensibly describes Applicants' invention, to "compile" generally means producing a machine

instruction version of human-readable program instructions. In a general context, to "compile" often means to aggregate or collect. It is not entirely clear whether this limitation requires "a collection" of a plurality of said functions, or whether it requires "a machine instruction version" of a plurality of said functions. For the purposes of examination, the term "to compile" will be interpreted as "to collect". Because of the computer software context of the invention, clarification of Applicants' use of this term is respectfully requested.

Claims 4 and 5 are difficult to interpret because they appear to define "a static load model" and "a dynamic callback function" as somehow analogous or similar. While dependent claims may present varied limitations, the nearly identical nature of these claims provide two alternate structures "wherein said parameter is provided through said user program." However, the Examiner see no link between "a static load model," understood to be an abstract or mathematical explanation of the behavior of an electronic circuit, and "a dynamic callback function," understood to be a software engineering construct for achieving communication between software components. The Examiner submits that claim 5, in the absence of claim 4, provides the limitation most likely to be deemed as distinctly claiming the invention. It is not known what is meant by "providing a parameter through a user program by a static load model."

In claim 10, preamble states "a method of modeling and simulating a circuit" but recites limitations that fail to clearly define a method of modeling or simulating a circuit. It is unclear if this claim language renders the term "modeling" as synonymous with "simulating."

Claim 16 presents similar ambiguity.

Claim Rejections - 35 USC § 112

The previous rejections under 35 U.S.C. § 112 have been withdrawn.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1, 4-5, 7-8, 10, and 12-13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 4-5, and 7-8 are directed to "a computerized simulation system" comprising "a simulator module," "a code module," and "an interface." There is no requirement for any tangible hardware components in the claim. In light of the specification, which is primarily directed to computer software, claims 1, 4-5, and 7-8 define a computer *software* "system" and are therefore nonstatutory as reciting functional descriptive material *per se*. Please see MPEP 2106.

Claims 10 and 12-13 define a method that fails to produce a useful, concrete, and tangible result as established in MPEP 2106(II)(A). Although the recited steps fail to achieve either "simulating" or "modeling," these acts also fail to produce a useful, concrete, and tangible result in isolation. In light of the specification, which is primarily directed to computer software, the recited steps of "adding an interface to said code module," and "assigning inputs, outputs, and load parameters," etc., define steps of a nonstatutory software method. In order for such a

method to meet the requirements of 35 U.S.C. § 101, the method must be limited to a practical application and it must produce a useful, concrete, and tangible result.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Claim Interpretation

Because of the 35 U.S.C. § 112 rejections, the claims are so indefinite and incomplete that no art rejection would be warranted as substantial guesswork would be involved in determining the scope and content of these claims. See *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962); *Ex parte Brummer*, 12 USPQ 2d, page 1654; and also *In re Wilson*, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). However, in the interest of compact prosecution, an art rejection will be asserted in view of the broadest and most reasonable interpretation of the claims. *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

Claims 1-20 are interpreted as a circuit simulator implemented on a computer system including a user interface.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

3. Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,077,304 to Kasuya (Kasuya) in view of "How Computers Work, 6th Edition" by Ron White (White), further in view of "IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition" (IEEE), further in view of "Microsoft Computer Dictionary, Fifth Edition" (Microsoft).

Kasuya discloses a circuit simulator implemented on a computer system including a user interface [Fig. 2, reference 102 "Verilog Circuit Simulator", reference 108 "CPU", reference 115 "User Interface"]. Further, Kasuya discloses an API to control the simulator [*"The HDL circuit simulator 102 includes an application program interface (API) 110 that enables other programs to control the operation of the HDL circuit simulator 102 through the use of pre-established instructions (actually procedure calls)."* (column 4, lines 7-11)].

White discloses various basic concepts that are fundamental to modern computer systems, such as "dynamic link libraries (DLLs)" (page 62), and "*calling* a function" (page 62), "*return* information [from a DLL call]" (page 62).

IEEE discloses various definitions as known in the art, including *function* (def. 9 is the most relevant), and *application program interface (API)*.

Microsoft discloses various definitions as known in the art, including *dynamic-link library*.

It would have been obvious to a person of ordinary skill in the art of either software engineering or computer-implemented circuit simulation to combine basic concepts such as those found in "How Computers Work" or a dictionary to implement a computer program that simulates a circuit. Motivation to make those combinations would be found in the knowledge of a person of ordinary skill in the art as well as the nature of the problem to be solved. In this case, a person of ordinary skill is expected to be aware of the basic concepts of computer software. In this case, the problem to be solved is implementing computer software and therefore lends itself to a solution involving the basic concepts of computer software.

In response, Applicants argue primarily that:

> [The present invention] uses a novel means to record function calls and further compile those recorded calls into a library that represents a black box circuit (*cit. omitted*). The black box circuit can then be simulated independently or as a part of a larger circuit design. The user is unaware of any circuit details inside the black box circuit yet is still able to accomplish accurate simulation in a shorter period of time. None of the cited references teach a means for "secretly" modeling and simulating a circuit in such a way that the user cannot have access to the circuit details, and further, does not *need* access to perform an accurate simulation.

The Examiner respectfully traverses this argument as follows.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "novel means to record function calls," "compiling those recorded calls into a library that represents a black box circuit," "secretly modeling and simulating a circuit,") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

While the claims recite that "said function is recorded," this and similar recitations fall far short of representing Applicants' arguments regarding a black box circuit and secretly modeling and simulating a circuit.

However, to fully address the alleged deficiencies of the prior art, Applicants' attention is respectfully drawn to Kasuya, (column 4, lines 25-45, emphasis added):

> "The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL **circuit specification 106** received from the system's **user via a user interface procedure 114** that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115). **The simulation engine 112 simulates the operation of specific circuit components in accordance with predefined circuit models 116, typically stored in a library of such models.** The circuit models 116 define not only the functionality of the circuit components but the time domain and frequency domain transfer characteristics of each circuit component when manufactured using a particular circuit manufacturing process. The performance of the specified circuit as simulated by the simulation engine 112 is also determined by the waveforms of the specified circuit's input signals. **The input signal waveforms can be specified by the user via the user interface 114, 115**, or can

> be specified through the API 110 through the use of predefined procedure calls for defining input signal waveforms."

Thus Kasuya teaches "a library that represents a black box circuit," specifically *predefined circuit models 116, typically stored in a library of such models.*

Applicants further argue primarily that:

> Furthermore, the present invention is not limited to simulating a particular electrical or environmental parameter for a circuit, but rather can simulate any conceivable input, output, and/or load parameter that has been converted to a computer readable format, without having to change simulators (*cit. omitted*). The enhanced accuracy of the methodology stems from the method's ability to instantaneously calculate any parameter value at any node of a circuit using input, output, and loading parameters simultaneously.

The Examiner respectfully traverses this argument as follows.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "simulate[ing] any conceivable input, output, and/or load parameter," "instantaneously calculate[ing] any parameter value at any node of a circuit using input, output, and loading parameters simultaneously") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

While these limitations are not recited in the claims that are not subject to restriction requirement, Applicants are advised that limitations such as "simulating <u>any conceivable input</u>" or "<u>instantaneously calculating any parameter value at any node of a circuit</u>" will draw special scrutiny regarding the requirements of 35 U.S.C. § 112, first paragraph, for adequate written description and enabling support.

Applicants' arguments have been fully considered but have been found unpersuasive.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
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Paul L. Rodriguez 2/2/06
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